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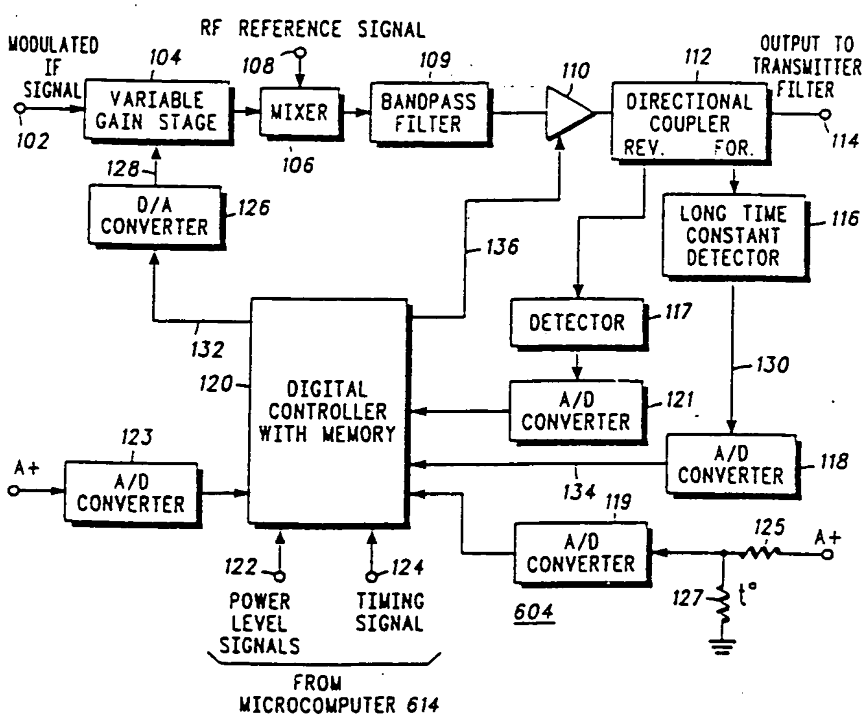
(54) Title: POWER CONTROL CIRCUITRY FOR A TDMA RADIO FREQUENCY TRANSMITTER

(57) Abstract

A transmitter (604) of a TDMA cellular telephone (600) includes power control circuitry having a variable gain stage (104). In operation, the variable gain stage (104) is responsive to a gain control signal (128) for adjusting a modulated IF signal. The temperature and supply voltage are sampled by controller (120) at the beginning of each time slot. Adjustments in the gain control signal (128) dictated by the sampled temperature and supply voltage are made by controller (120) in each time slot prior to keying the RF amplifier (110). The transmit RF signal is amplified by the RF amplifier (110) to produce the transmit output signal. The forward power and reverse power of the transmit output signal are sampled by controller (120) at the end of each time slot. The sampled forward power is used by controller (120) in calculating the value of the gain control signal for the next time slot. If the sampled reverse power or supply voltage exceed respective maximum values, the RF amplifier (110) is dekeyed by controller (120).



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POWER CONTROL CIRCUITRY FOR A TDMA RADIO FREQUENCY TRANSMITTER

Related Applications

This application is related to the instant assignee's copending application, serial no. 07/632,231, filed December 20, 1990, invented by Thomas J. Walczak and Stephen V. Cahill, and entitled "Power Control Circuitry for a TDMA Radio Frequency Transmitter".

Background of the Invention

The present invention is generally related to radiotelephones, and more particularly to a power control circuitry for a radio frequency (RF) transmitter operating in a continuous mode or a time-division multiple-access (TDMA) mode, that may be advantageously used in dual-mode digital/analog cellular telephones.

Analog cellular telephones currently are continuously transmitting during a telephone call. RF transmitters of such analog cellular telephones are frequency modulated with voice signals and continuously operated at one of eight different power levels depending the quality of the RF signal received therefrom by the cellular system base station. The output power of such RF transmitters are maintained at the desired power level by conventional automatic output power control circuitry, such as, for example, the circuitry shown and described in U.S. Patent No. 4,523,155.

However, such conventional output power control circuitry is inadequate for TDMA cellular systems where it is necessary to rapidly pulse the RF transmitter on for 6.67 milliseconds and off 13.33 milliseconds every 20 milliseconds. Furthermore, it is also necessary that the RF transmitter

output follow the envelope of the modulation, which has frequency components in excess of 12.15 KHz. These problems may be solved in part by output power control circuitry employing variable attenuators which attenuate the RF input to the transmitter power amplifier. An example of such output power control circuitry employing a variable attenuator is shown and described in U.S. Patent No. 4,803,440. However, when such output power control circuitry is operated with a linear power amplifier at cellular transmitter frequencies ranging from 824 MHz to 849 MHz, output power can not be accurately maintained initially and dynamically due to resulting performance degradations, such as power amplifier saturation caused by temperature or supply voltage variations, inaccurate initial power levels caused by temperature, and incorrect power levels caused by antenna loading variations. For the foregoing reasons, there is a need for improved power control circuitry for precisely maintaining initially and dynamically the RF output signal from a TDMA RF signal transmitter at one of a plurality of power levels selected by the level control signals over temperature variations, supply voltage variations, and antenna loading variations.

Summary of the Invention

Briefly stated, the present invention encompasses novel power control circuitry responsive to a transmit signal, level control signals, a timing signal defining a series of transmit time intervals, and a supply voltage from a signal source for maintaining during the transmit time intervals the average magnitude of a radio frequency (RF) output signal at a power level selected from a plurality of power levels by the level control signals. The power control circuitry comprises: memory circuitry for storing the value of a gain control signal; adjusting circuitry having variable gain for adjusting the

transmit signal during the transmit time intervals substantially in proportion to the the stored value of the gain control signal to produce an adjusted transmit signal; amplifying circuitry coupled to the supply voltage for amplifying the transmit signal to produce the RF output signal; antenna circuitry coupled to the amplifying means for transmitting the RF output signal; voltage detecting circuitry for detecting the magnitude of the supply voltage; temperature detecting circuitry for detecting the temperature of the power control circuitry; power detecting circuitry coupled to the RF output signal for generating an output signal having a value related to the magnitude of the forward power of the RF output signal; and control circuitry coupled to the power detecting circuitry for sampling the value of the output signal substantially at the end of each transmit time interval, adjusting the value of the gain control signal in response to the difference between the sampled value of the output signal and the selected power level, and storing the adjusted value of the gain control signal in the memory means, said control circuitry further being coupled to the temperature detecting circuitry for adjusting the gain control signal by a first predetermined amount substantially at the beginning of each transmit time interval when the detected temperature is greater than a predetermined temperature, and said control circuitry further being coupled to the voltage detecting circuitry for adjusting the gain control signal by a second predetermined amount substantially at the beginning of at least the initial transmit time interval when the detected magnitude of the supply voltage is less than a predetermined magnitude.

Brief Description of the Drawings

FIG. 1 is a block diagram of a TDMA cellular telephone, which may advantageously utilize the power control circuitry of the present invention, as embodied preferably in FIG. 2.

FIG. 2 is a block diagram of power control circuitry for an RF transmitter of TDMA cellular telephone 600 in FIG. 1, embodying the present invention.

FIG. 3 is a timing diagram for the power control circuitry in FIG. 2.

FIG. 4 is a circuit diagram of long time constant detectors 116 and 117 in FIG. 2.

FIG. 5 is a circuit diagram of directional coupler 112 in FIG. 2.

FIG. 6 is a flow chart for the process used by controller 120 in FIG. 2.

FIG. 7 is a flow chart for the initial output power control calculation routine 308 used by controller 120 in FIG. 2.

FIG. 8 is a flow chart for the continuous output power control calculation routine 307 used by controller 120 in FIG. 2.

FIG. 9 is a flow chart for the output power detection routine 314 used by controller 120 in FIG. 2.

Description of the Preferred Embodiment

Referring to FIG. 1, there is illustrated a block diagram of a TDMA cellular telephone 600 suitable for use in dual-mode TDMA/FDMA cellular telephones, which may advantageously utilize the power control circuitry of the present invention, as embodied preferably in FIG. 2. Telephone 600 includes, in its transmit signal path, microphone 608, vocoder 612, data format circuitry 601, quadrature modulator 602, 90 MHz local oscillator 606, transmitter with mixer 604, transmitter filter 618, and antenna 620. In its receive signal path, telephone 600

includes antenna 620, receiver filter 622, quadrature demodulator 624, data deformat circuitry 625, vocoder 612, and speaker 610. The channel frequency of telephone 600 is loaded into synthesizer 616 by microcomputer 614 and applied to transmitter 604 and demodulator 624. In the preferred embodiment, the duplex radio channels have transmit frequencies in the range from 824 MHz to 849 MHz and receive frequencies in the range from 869 MHz to 894 MHz. Telephone 600 is controlled by microcomputer 614 which includes a memory with a control and signaling computer program stored therein. In the preferred embodiment of telephone 600, microcomputer 614 is implemented with commercially available microcomputers, such as, for example, the Motorola type 68HC11 microcomputer. Although cellular telephone 600 utilizes TDMA RF channels, the present invention may also be utilized in conventional frequency division multiple access cellular telephones, in code division multiple access cellular telephones, and in other analog and digital cellular telephones employing different transmission schemes.

In the preferred embodiment of telephone 600 in FIG. 1, quadrature modulator 602 may be implemented as described in the instant assignee's US patent no. 5,020,076, entitled "Hybrid Modulation Apparatus", invented by Stephen V. Cahill et al., and granted May 28, 1991 (incorporated herein by reference). Quadrature modulator 602 modulates TDMA RF signals with voice, data and signalling information according to π/4-shift differential quadrature phase shift keying (DQPSK). DQPSK modulation is described in "Digital Communications", by John G. Proakis, 1st Ed., ISBN 0-07-050927-1, at pages 171-178. Data format circuitry 601 combines the output of vocoder 612 with signalling and overhead information and encodes the result according to π/4-shift DQPSK modulation into the transmit I and Q signals. The π/4-shift DQPSK modulation and signalling information is

specified in Interim Standard 54 published by and available from the Electronic Industries Association, Engineering Department, 2001 Eye Street N.W., Washington, D.C. 20006.

The signal vector representing the $\pi/4$-shift DQPSK modulation consists of a cosine component and a sine component. The signal scaling the amplitude of the cosine component is also known as the in-phase or I signal and the signal scaling the amplitude of the sine component is also known as the quadrature or Q signal. The I and Q scaled cosine and sine signals are the orthogonal quadrature components at the frequency of the 90 MHz signal from local oscillator 606; the modulated transmit IF signal 102 then being created by adding the I and Q signals.

Symbols representing the vector components of the I and Q signals are generated in data format circuitry 601 by shifting the vector components such that phase shifts of IF signal 102 of $\pm\pi/4$ or $\pm 3\pi/4$ radians are generated. Each phase shift encodes one of four possible symbols.

Serial digital data from vocoder 612 that is eventually to be modulated by modulator 602 is first converted to bit pairs in data format circuitry 601. Each bit pair specifies a symbol that is the desired vector shift relative to the previously transmitted symbol. The mapping of bit pairs to symbol vectors is according to the equations:

$$I(k) = I(k-1)\cos(\Delta\phi(X(k),Y(k)))-Q(k-1)\sin(\Delta\phi(X(k),Y(k)))$$
$$Q(k) = I(k-1)\sin(\Delta\phi(X(k),Y(k)))+Q(k-1)\cos(\Delta\phi(X(k),Y(k)))$$

where k is an index of the bit pairs; k=1 for bits one and two paired, k=2 for bits three and four paired, etc. I(k-1) and Q(k-1) are the amplitudes of the cosine and sine components of the previous symbol vector. X(k) represents the first bit of bit pair (k) and Y(k) represents the second bit of bit pair (k). The phase change, $\Delta\phi$, is determined according to the following table:

X(k)	Y(k)	Δø(X(k),Y(k))
1	1	$-3\pi/4$
0	1	$3\pi/4$
0	0	$\pi/4$
1	0	$-\pi/4$

Thus, one of four possible symbols are transmitted for each two bits of the serial data stream.

The reason for the modulation nomenclature $\pi/4$-shift DQPSK and how it works is now evident: the phase shift is in $\pi/4$ increments in vector space, symbols are differentially encoded with respect to the previous symbol vector, and the information bearing quantity in IF signal 102 is the phase-shift with one of four possible shifts between any two symbols. The operation of modulator 602 is represented by the equation:

$$V_{out}(t)= (I(t))\cos(2\pi ft)+(Q(t))\sin(2\pi ft)$$

where $V_{out}(t)$ is the modulated IF signal 102 and I(t) and Q(t) are I(k) and Q(k) as defined above as a function of time, and f is the transmit IF of 90 MHz.

In the preferred embodiment of telephone 600 in FIG. 1, quadrature demodulator 624 may be implemented as described in the instant assignee's copending patent application no. 07/590,401, entitled "A Carrier Recovery Method and Apparatus Having an Adjustable Response Time Determined by Carrier Signal Parameters", invented by Stephen V. Cahill, and filed 28 September, 1990 (incorporated herein by reference). Quadrature demodulator 624 demodulates TDMA RF signals modulated with information according to $\pi/4$-shift DQPSK and generates the receive I and Q signals. The receive I and Q signals are deformated and decoded by data deformat

circuitry 625 to recover the digitized voice signals, which are applied to vocoder 612.

In the preferred embodiment of telephone 600 in FIG. 1, vocoder 612 is implemented as described in the instant assignee's US patent nos. 4,817,157 and 4,896,361 (incorporated herein by reference). Vocoder 612 encodes and decodes voice signals according to code excited linear prediction (CELP) coding. Filters 618 and 622 are intercoupled as a duplexer for transmitting TDMA RF signals on, and receiving TDMA RF signals from antenna 620. Filters 618 and 622 may be any suitable conventional filters, such as, for example, the filters described in US patent nos. 4,431,977, 4,692,726, 4,716,391, and 4,742,562 (incorporated herein by reference). Vocoder 612, data format circuitry 601, data deformat circuitry 625, quadrature modulator 602, and quadrature demodulator 624 may be implemented with commercially available digital signal processors, such as, for example, the Motorola type DSP 56000 digital signal processor.

According to the present invention, power control circuitry of transmitter 604 in FIG. 1 is preferably implemented as illustrated in FIG. 2. Although utilized in telephones 600, the power control circuitry of the present invention may also be utilized in dual-mode TDMA/FDMA cellular telephones, conventional frequency division multiple access cellular telephones, in code division multiple access cellular telephones, and in other analog and digital cellular telephones employing different transmission schemes. Referring now to FIG. 2, the power control circuitry includes variable gain stage 104, mixer 106, bandpass filter 109, RF amplifier 110, and directional coupler 112 in a forward path, and detectors 116 and 117, analog-to digital (A/D) converters 118, 119, 121 and 123, digital controller 120 and digital-to analog (D/A) converter 126 in a feedback path. Transmit IF

signal 102 from quadrature modulator 602 has a frequency of 90 MHz and is modulated with DQPSK information.

Stage 104 in FIG. 2 has a variable gain for adjusting the magnitude of IF signal 102 in response to a gain control signal, D/A converter output signal 128. Stage 104 may be implemented by means of a variable gain amplifier or a variable gain attenuator, where the gain is adjusted substantially in proportion to the value of gain control signal 128. In the preferred embodiment, stage 104 is a variable gain amplifier similar to the Motorola type MC1350 IF amplifier. The adjusted IF signal from stage 104 is mixed with the RF reference signal 108 from synthesizer 616 to produce the RF transmit signal. The RF transmit signal is filtered by bandpass filter 109 and amplified by RF amplifier 110, and passed through directional coupler 112 to produce the RF transmit output signal 114. The transmit output signal 114 is coupled from directional coupler 112 to transmit filter 618 and thereafter antenna 620 for transmission.

The operation of the power control circuitry in FIG. 2 is further illustrated by the timing diagram in FIG. 3. Timing signal 124 has a waveform defining a series of transmit time intervals, which in FIG. 3 correspond to time slot TS1 of three possible time slots TS1, TS2, and TS3 for a TDMA RF channel. The TDMA RF channel consists of multiple frames of 20 milliseconds each containing three time slots TS1, TS2, and TS3 of approximately 6.67 milliseconds each. During a cellular telephone call in a TDMA cellular system, TDMA cellular cellular telephone 600 is assigned to a TDMA RF channel and a time slot of that channel for transmission of the modulated transmit output signal 114 carrying voice signals, signalling information and overhead information. Accordingly, it is necessary that the transmit output signal 114 be transmitted, over varying A+ supply voltage, temperature and antenna loading, at the desired power level

selected by the power level signals 122 during each of the assigned time slots.

In the power control circuitry in FIG. 2, D/A converter 126 is loaded by controller 120 at the beginning of each assigned time slot with the value stored in its memory and at the end of each assigned time slot with a zero value for essentially turning the transmit output signal 114 on and off. In addition, amplifier 110 may also be turned on and off by gating its bias on and off by way of bias control signal 136. The D/A converter output 128 in FIG. 2 has a value which varies from time slot to time slot to maintain the output power of transmit output signal 114 at the desired power level. The waveform of detector output 130 in FIG. 2 has an exponential response due to the relatively long time constant of detector 116 with respect to the time slot length. Due to the relatively long time constant of detector 116, the output of detector 116 near the end of the time slot has a value related to the average magnitude of the transmit output signal 114. Detectors 116 and 117, as shown in FIG. 4, include rectifying circuitry comprised of diode 502 and capacitor 504, and averaging circuitry comprised of capacitors 504 and 508 and resistor 506. In the preferred embodiment, averaging circuitry 504, 506 and 508 has a time constant of approximately one millisecond.

Near the end of each time slot as illustrated by the sample times in FIG. 3, the value of the detector output 130 is sampled via A/D converter 118 and used by controller 120 to compute a new value of D/A converter output 128 by subtracting the sampled value (DETECT in FIG. 8 and 9) of the detector output 130 from the desired value for the selected power level, scaling the difference by a pre-selected factor, and summing the scaled difference with the previous value stored in memory. The new value of D/A converter output 128 is stored by controller 120 in its memory and loaded into D/A converter 126 at the beginning of the next assigned time slot.

According to a feature of the present invention, the magnitude of the A+ supply voltage and the magnitude of the temperature of the power control circuitry as reflected by the magnitude of thermistor 127 (located in the same housing as RF amplifier 110) are sampled by A/D converters 123 and 119, respectively, and used by controller 120 together with the magnitude of the forward power as sampled by A/D converter 118 for accurately and reliably maintaining the output power of the transmit output signal 114 at the desired one of the possible eight power levels. In the preferred embodiment, the desired power level must be maintained within +2 to -4 dB of the nominal power for that power level (see the aforementioned Interim Standard 54). Since RF amplifier 110 is preferably a linear power amplifier for TDMA operation of telephone 600, it is susceptible to three undesirable operating conditions: (1) saturation due to low A+ supply voltage or high temperature; (2) low or high initial output power levels due to temperature induced gain changes; or (3) excessive reflected power due to a damaged, missing, or obstructed antenna. Operating RF amplifier under such undesirable conditions may result in poor linearity causing interference with other cellular radio channels. By utilizing the present invention, the output power of transmit output signal 114 is maintained at the desired power level by monitoring not only the magnitude of the forward power, but also the magnitude of A+ supply voltage and temperature of the power control circuitry, and appropriately adjusting the D/A converter output 128 in response to the changes detected in same. Moreover, if the A+ supply voltage exceeds a predetermined maximum voltage VMAX, or if the reverse power is outside its normal range, the RF amplifier 110 is dekeyed (i.e. shut off by gating off its bias by way of bias control signal 136) to protect it from damage.

Referring next to FIG 6, there is illustrated a flow chart for the process used by controller 120 for maintaining the

output power of the transmit output signal 114 at the desired power level. At the beginning of the current transmission, the bias of RF amplifier 110 is gated on by way of bias control signal 136. Entering at START block 302, the process proceeds to decision block 304, where a check of timing signal 124 is made to determine if timing signal 124 has a binary one state. If not, NO branch is taken to wait. If timing signal 124 has a binary one state, YES branch is taken from decision block 304 to block 306, where a check of is made to determine if transmitter 604 is initially being keyed up (i.e., turned on) or if a power step change must be made. If so, YES branch is taken to block 308 where the initial output power control calculation routine in FIG. 7 is executed. If transmitter 604 is not being initially keyed up or a power step change need not be made, NO branch is taken from decision block 306 to block 307 where the continuous output power control calculation routine in FIG. 8 is executed. Execution of the routines in FIG. 7 or 8 determines the value for D/A converter output 128. Next, at block 310, the determined value AOCCNT for D/A converter output signal 128 is applied to D/A converter 126 for keying up RF amplifier 110. D/A converter 126 in turn converts the applied value AOCCNT to an analog gain control voltage, which is applied to variable gain stage 104 for adjusting the amount of gain.

Next, at decision block 312 in FIG 6, a check of timing signal 124 is made again to determine if the timing signal 124 has a binary zero state. If not, NO branch is taken to wait. If timing signal 124 has a binary zero state, YES branch is taken from decision block 312 to block 314, where the output power detection routine in FIG. 9 is executed. Execution of the routines in FIG. 9 determines the value for the forward power DETECT and the value for the reverse power REVERSE POWER. Next, at block 316, transmitter 604 is dekeyed (i.e., shut off) by setting D/A converter output 128 to zero. Then, at

block 318, a new value of D/A converter output 128 is calculated by subtracting the sampled value of the detector output 130 from the desired value for the selected power level, scaling the difference by a pre-selected factor, and summing the scaled difference with the previous value of D/A converter output 128 stored in memory. Then, the new value of D/A converter output 128 is stored in the memory of controller 120 at block 320 for use during the next assigned time slot, and control returns to decision block 304 to repeat the foregoing process for the next assigned time slot. At the end of the current transmission, the bias of RF amplifier 110 is gated off by way of bias control signal 136.

Referring next to FIG 7, there is illustrated a flow chart for the initial output power control calculation routine 308 in FIG.6 used by controller 120 in FIG. 2. Entering at START block 702, the process proceeds to block 704 where the output of A/D converter 123 is read and stored in the location labelled A+. Next, at decision block 706, a check is made to determine if the value of A+ is greater than VMAX, which is a predetermined A/D converter output value corresponding to the maximum allowable A+ voltage. If so, YES branch is taken to block 708 to dekey RF amplifier 110 and set the FAIL FLAG to a binary one state, and thereafter program control proceeds to END block 710 to terminate further operation of RF amplifier 110. If A+ is not greater than VMAX, NO branch is taken from decision block 706 to block 712, where AOCCNT is set to the values for the selected power step stored in a table in the memory of controller 120. The table in the memory of controller 120 stores phased D/A converter values for each of the eight power steps. The stored values when applied to D/A converter 128 produce the desired initial magnitude of output power of the transmit output signal 114.

Next, at block 714, the value of the output of A/D converter 119 is read by controller 120 and stored in the

variable TH. A/D converter 119 samples the voltage across thermistor 127, which is coupled to the A+ supply voltage by resistor 125. The magnitude of the voltage across thermistor 127 is proportional to the temperature of the power control circuitry. Next, at decision block 716, a check is made to determine if the value of TH is greater than THOT, which is a predetermined A/D converter output value corresponding to the high temperature operating range of RF amplifier 110. If so, YES branch is taken to block 724 where AOCCNT is set to its previous value minus KHOT, which is a predetermined A/D converter output value corresponding to a gain adjustment constant for high temperature operation of RF amplifier 110. Although AOCCNT is adjusted in blocks 719, 722, 724, 728 and 732 of FIG. 7 and in blocks 822, 824, 828 and 832 of FIG. 8, in other embodiments, the selected power level PLEVEL may be temporarily adjusted instead of AOCCNT, provided that the initial values of the eight power levels are not changed. Next, at decision block 726, a check is made to determine if the value of A+ is less than VHSATX, which is a predetermined A/D converter output value corresponding to the A+ supply voltage at which RF amplifier 110 enters saturation at high temperature operation and the selected power step. If not, NO branch is taken to RETURN block 734 to return to the flow chart of FIG. 6. If A+ is less than VHSATX, YES branch is taken from decision block 726 to block 728, where AOCCNT is set to its previous value minus KHSATX, which is a predetermined A/D converter output value corresponding to a voltage margin that will prevent saturation of RF amplifier 110 at high temperature operation. Thereafter, program control returns to FIG. 6 at RETURN block 734.

Returning to decision block 716 in FIG. 7, if TH is not greater than THOT, NO branch is taken to decision block 718, where a check is made to determine if the value of TH is less

than TCOLD, which is a predetermined A/D converter output value corresponding to the low temperature operating range of RF amplifier 110. If so, YES branch is taken to block 719 where AOCCNT is set to its previous value minus KCOLD, which is a predetermined A/D converter output value corresponding to a gain adjustment constant for low temperature operation of RF amplifier 110. Next, at decision block 720, a check is made to determine if the value of A+ is less than VCSATX, which is a predetermined A/D converter output value corresponding to the A+ supply voltage at which RF amplifier 110 enters saturation at low temperature operation and the selected power step. If not, NO branch is taken to RETURN block 734 to return to the flow chart of FIG. 6. If A+ is less than VCSATX, YES branch is taken from decision block 720 to block 722, where AOCCNT is set to its previous value minus KCSATX, which is a predetermined A/D converter output value corresponding to a voltage margin that will prevent saturation of RF amplifier 110 at low temperature operation. Thereafter, program control returns to FIG. 6 at RETURN block 734. Returning to decision block 718, if TH is not less than TCOLD, NO branch is taken to decision block 730, where a check is made to determine if the value of A+ is less than VSATX, which is a predetermined A/D converter output value corresponding to the A+ supply voltage at which RF amplifier 110 enters saturation at normal temperature operation and the selected power step. If not, NO branch is taken to RETURN block 734 to return to the flow chart of FIG. 6. If A+ is less than VSATX, YES branch is taken from decision block 730 to block 732, where AOCCNT is set to its previous value minus KSATX, which is a predetermined A/D converter output value corresponding to a voltage margin that will prevent saturation of RF amplifier 110 at normal temperature operation. Thereafter, program control returns to FIG. 6 at RETURN block 734.

Referring next to FIG 8 , there is illustrated a flow chart for the continuous output power control calculation routine 307 in FIG.6 used by controller 120 in FIG. 2. Entering at START block 802, the process proceeds to block 804 where the output of A/D converter 123 is read and stored in the location labelled A+. Next, at decision block 806, a check is made to determine if the value of A+ is greater than VMAX, which is a predetermined A/D converter output value corresponding to the maximum allowable A+ voltage. If so, YES branch is taken to block 808 to dekey RF amplifier 110 and set the FAIL FLAG to a binary one state, and thereafter program control proceeds to END block 810 to terminate further operation of RF amplifier 110. If A+ is not greater than VMAX, NO branch is taken from decision block 806 to block 812, where AOCCNT is calculated from its previous value and the value of DETECT stored in the memory of controller 120. In the preferred embodiment, the new value of AOCCNT is calculated by subtracting the value of DETECT from the desired value for the selected power level PLEVEL, scaling the difference by a preselected factor KDET, and summing the scaled difference with the previous value of AOCCNT. This calculation is expressed in the following equation.

$$AOCCNT = AOCCNT + KDET(PLEVEL - DETECT)$$

Next, at decision block 814 in FIG. 8, the value of the output of A/D converter 119 is read by controller 120 and stored in the variable TH. Then, at decision block 816, a check is made to determine if the value of TH is greater than THOT. If so, YES branch is taken to block 824 where AOCCNT is set to its previous value minus KHOT. Next, at decision block 826, a check is made to determine if the value of A+ is less than VHSATX. If not, NO branch is taken to RETURN block 834 to return to the flow chart of FIG. 6. If A+ is less than VHSATX, YES branch is taken from decision block 826 to block 828, where AOCCNT is set to its previous value minus KHSATX.

Thereafter, program control returns to FIG. 6 at RETURN block 834.

Returning to decision block 816 in FIG. 8, if TH is not greater than THOT, NO branch is taken to decision block 818, where a check is made to determine if the value of TH is less than TCOLD. If so, YES branch is taken to block 819 where AOCCNT is set to its previous value minus KCOLD. Next, at decision block 820, a check is made to determine if the value of A+ is less than VCSATX. If not, NO branch is taken to RETURN block 834 to return to the flow chart of FIG. 6. If A+ is less than VCSATX, YES branch is taken from decision block 820 to block 822, where AOCCNT is set to its previous value minus KCSATX. Thereafter, program control returns to FIG. 6 at RETURN block 834. Returning to decision block 818, if TH is not less than TCOLD, NO branch is taken to decision block 830, where a check is made to determine if the value of A+ is less than VSATX. If not, NO branch is taken to RETURN block 834 to return to the flow chart of FIG. 6. If A+ is less than VSATX, YES branch is taken from decision block 830 to block 832, where AOCCNT is set to its previous value minus KSATX. Thereafter, program control returns to FIG. 6 at RETURN block 834.

Referring next to FIG 9, there is illustrated a flow chart for the output power detection routine 314 in FIG.6 used by controller 120 in FIG. 2. Entering at START block 902, the process proceeds to block 904 where the output of A/D converter 123 is read and stored in the location labelled A+. Next, at decision block 906, a check is made to determine if the value of A+ is greater than VMAX, which is a predetermined A/D converter output value corresponding to the maximum allowable A+ voltage. If so, YES branch is taken to block 916 to dekey RF amplifier 110 and set the FAIL FLAG to a binary one state, and thereafter program control proceeds to END block 918 to terminate further operation of RF amplifier 110.

Returning to decision block 906 in FIG. 9, if A+ is not greater than VMAX, NO branch is taken to block 908, where the output of A/D converter 118 is read and stored in the location labelled DETECT. Next, at block 910, the output of A/D converter 121 is read and stored in the location labelled REVERSE POWER. Then, at decision block 906, a check is made to determine if the value of REVERSE POWER is within the NORMAL RANGE, that is at least 10 dB less than the selected power level PLEVEL. If not, NO branch is taken to block 916 to dekey RF amplifier 110 and set the FAIL FLAG to a binary one state, and thereafter program control proceeds to END block 918 to terminate further operation of RF amplifier 110. If REVERSE POWER is within the NORMAL RANGE, YES branch is taken from decision block 912 to to RETURN block 914 to return to the flow chart of FIG. 6.

For the flow charts of FIG. 6, 7, 8 and 9, exemplary values of the variables used therein are set out below. These exemplary values are converted to A/D converter values and stored in the memory of controller 120.

PLEVEL = 7 dBm, 11 dBm, 15 dBm, 19 dBm,
23 dBm, 27 dBm, 31 dBm, or 35 dBm
TH = -30 to +60 Degrees Centigrade
A+ = 10.8 to 16.0 Volts
TCOLD = 0 Degrees Centigrade
THOT = +40 Degrees Centigrade
KHOT = 20 Millivolts
KCOLD = 20 Millivolts
VMAX = 15.0 Volts
VCSATX = 13.0 Volts
VHSATX = 11.0 Volts
VSATX = 12.0 Volts
KCSATX = 20 Millivolts
KHSATX = 20 Millivolts
KSATX = 20 Millivolts

ORMAL RANGE = At least 10 dB less than PLEVEL

summary, unique output power control circuitry maintains initially and dynamically the output transmit output signal at a desired power level ›y power level signals during a series of transmit time such as, for example, the assigned time slots of a channel. In operation, a variable gain stage is to a gain control signal for adjusting a modulated which is then mixed with an RF reference signal to ie transmit RF signal. The temperature and supply sampled at the beginning of each time slot. ts in the gain control signal dictated by the sampled e and supply voltage are made in each time slot ing the RF amplifier. The transmit RF signal is y an RF amplifier to produce the transmit output h is coupled by a directional coupler and transmit antenna for transmission. The forward power and er of the transmit output signal are sampled at the time slot. The sampled forward power is used in he value of the gain control signal for the next the sampled reverse power or supply voltage ctive maximum values, the RF amplifier is ie novel output power control circuitry of the ition may be advantageously utilized in TDMA hones as well as in dual-mode TDMA/FDMA hones, conventional frequency division multiple r telephones, code division multiple access iones, and other analog and digital radio iploying different transmission schemes.

power detecting
›ut signal
interval,
in response to the
irst output signal
adjusted value of
s, said control
ture detecting
›y a first
beginning of each
mperature is
and said control
detecting means for
id predetermined
least the initial
nagnitude of the
d magnitude.

ccording to claim 1,
means coupled to
›nd output signal
f the reverse power of
further being
ans for disabling the
second output signal

according to claim 2,
neans for coupling a
itput signal to the

y according to claim 1,
nalog to digital

NORMAL RANGE = At least 10 dB less than PLEVEL

In summary, unique output power control circuitry ›recisely maintains initially and dynamically the output ·ower of transmit output signal at a desired power level elected by power level signals during a series of transmit time ıtervals, such as, for example, the assigned time slots of a 'DMA RF channel. In operation, a variable gain stage is esponsive to a gain control signal for adjusting a modulated F signal, which is then mixed with an RF reference signal to roduce the transmit RF signal. The temperature and supply oltage are sampled at the beginning of each time slot. djustments in the gain control signal dictated by the sampled mperature and supply voltage are made in each time slot rior to keying the RF amplifier. The transmit RF signal is nplified by an RF amplifier to produce the transmit output gnal which is coupled by a directional coupler and transmit ter to an antenna for transmission. The forward power and verse power of the transmit output signal are sampled at the ıd of each time slot. The sampled forward power is used in lculating the value of the gain control signal for the next me slot. If the sampled reverse power or supply voltage ceed respective maximum values, the RF amplifier is keyed. The novel output power control circuitry of the esent invention may be advantageously utilized in TDMA llular telephones as well as in dual-mode TDMA/FDMA llular telephones, conventional frequency division multiple cess cellular telephones, code division multiple access llular telephones, and other analog and digital radio ephones employing different transmission schemes.

ans, digital
ng means,
gital
rting
r converting
mal, said
ut signal to
erating a
alog
ntrol signal

to claim 1,
coupling a
al to the first

to claim 1,
t diode
s comprises

to claim 1,
said antenna

ty of radio

ansmitting

nna means
ity of radio

transmitting means coupled to the antenna means for transmitting a radio frequency (RF) output via one of the plurality of radio channels, said transmitting further including power control circuitry responsive to a transmit signal, level control signals, a timing signal defining a series of transmit time intervals, and a supply voltage from a signal source for maintaining during the transmit time intervals the average magnitude of the RF output signal at a power level selected from a plurality of power levels by the level control signals, said supply voltage having a magnitude between a predetermined minimum voltage and a predetermined maximum voltage, said power control circuitry further comprising:

memory means for storing the value of a gain control signal;

adjusting means having variable gain for adjusting the transmit signal during the transmit time intervals substantially in proportion to the stored value of the gain control signal to produce an adjusted transmit signal, said adjusting means substantially blocking the transmit signal at times other than those during the transmit time intervals;

amplifying means coupled to the supply voltage for amplifying the transmit signal to produce the RF output signal;

voltage detecting means for detecting the magnitude of the supply voltage;

temperature detecting means for detecting the temperature of the power control circuitry;

power detecting means coupled to the RF output signal for generating an output signal having a value related to the magnitude of the forward power of the RF output signal; and

control means coupled to the power detecting means for sampling the value of the output signal substantially at the end of each transmit time interval, adjusting the value of the gain control signal in response to the difference between the sampled value of the output signal and the selected power level, and storing the adjusted value of the gain control signal in the memory means, said control means further being coupled to the temperature detecting means for adjusting the gain control signal by a first predetermined amount substantially at the beginning of each transmit time interval when the detected temperature is greater than a predetermined temperature, and said control means further being coupled to the voltage detecting means for adjusting the gain control signal by a second predetermined amount substantially at the beginning of of at least the initial transmit time interval when the detected magnitude of the supply voltage is less than a predetermined magnitude.

9. Power control circuitry responsive to a transmit intermediate frequency (IF) signal, level control signals, a timing signal defining a series of transmit time intervals, and a supply voltage from a signal source for maintaining during the transmit time intervals the average magnitude of a radio frequency (RF) output signal at a power level selected from a plurality of power levels by the level control signals, said supply voltage having a magnitude between a predetermined minimum voltage and a predetermined maximum voltage, said power control circuitry comprising:

reference means for generating an RF reference signal;

memory means for storing the value of a gain control signal;

adjusting means having variable gain for adjusting the transmit IF signal during the transmit time

intervals substantially in proportion to the stored value of the gain control signal to produce an adjusted transmit IF signal, said adjusting means substantially blocking the transmit IF signal at times other than those during the transmit time intervals;

mixing means for combining the adjusted transmit IF signal and the RF reference signal to produce an RF transmit signal;

amplifying means coupled to the supply voltage for amplifying the RF transmit signal to produce the RF output signal;

antenna means coupled to the amplifying means for transmitting the RF output signal;

voltage detecting means for detecting the magnitude of the supply voltage;

temperature detecting means for detecting the temperature of the power control circuitry;

first power detecting means coupled to the RF output signal for generating a first output signal having a value related to the magnitude of the forward power of the RF output signal; and

control means coupled to the first power detecting means for sampling the value of the first output signal substantially at the end of each transmit time interval, adjusting the value of the gain control signal in response to the difference between the sampled value of the first output signal and the selected power level, and storing the adjusted value of the gain control signal in the memory means, said control means further being coupled to the temperature detecting means for adjusting the gain control signal by a first predetermined amount substantially at the beginning of each transmit time interval when the detected temperature is greater than a predetermined temperature, and said control means further being coupled to the voltage detecting means for

adjusting the gain control signal by a second predetermined amount substantially at the beginning of of at least the initial transmit time interval when the detected magnitude of the supply voltage is less than a predetermined magnitude.

10. The power control circuitry according to claim 9, further including second power detecting means coupled to the RF output signal for generating a second output signal having a value related to the magnitude of the reverse power of the RF output signal, said control means further being coupled to the second power detecting means for disabling the amplifying means when the value of the second output signal exceeds a predetermined value.

11. The power control circuitry according to claim 10, further including directional coupling means for coupling a portion of the reverse power of the RF output signal to the second detecting means.

12. The power control circuitry according to claim 9, wherein said control means includes analog to digital converting means coupled to the first detecting means, digital to analog converting means coupled to the adjusting means, and processing means coupled to said analog to digital converting means and said digital to analog converting means, said analog to digital converting means for converting the first output signal to a digitized first output signal, said processing means sampling the digitized first output signal to sample the value of the first output signal and generating a digitized gain control signal, and said digital to analog converting means converting the digitized gain control signal to the gain control signal.

13. The power control circuitry according to claim 9, further including directional coupling means for coupling a portion of the forward power of the RF output signal to the first detecting means.

14. The power control circuitry according to claim 9, wherein said first detecting means comprises first diode detecting means and said second detecting means comprises second diode detecting means.

15. The power control circuitry according to claim 9, further including filtering means intercoupling said antenna means and said amplifying means.

16. A radio communicating via a plurality of radio channels, said radio comprising in combination:

antenna means for receiving and transmitting signals via the plurality of radio channels;

receiving means coupled to the antenna means for receiving a receive signal via one of the plurality of radio channels;

transmitting means coupled to the antenna means for transmitting a radio frequency (RF) output via one of the plurality of radio channels, said transmitting further including power control circuitry responsive to a transmit intermediate frequency (IF) signal, level control signals, a timing signal defining a series of transmit time intervals, and a supply voltage from a signal source for maintaining during the transmit time intervals the average magnitude of the RF output signal at a power level selected from a plurality of power levels by the level control signals, said supply voltage having a magnitude between a predetermined minimum voltage and a predetermined maximum voltage, said power control circuitry further comprising:

reference means for generating an RF reference signal;

memory means for storing the value of a gain control signal;

adjusting means having variable gain for adjusting the transmit IF signal during the transmit time intervals substantially in proportion to the stored value of the gain control signal to produce an adjusted transmit IF signal, said adjusting means substantially blocking the transmit IF signal at times other than those during the transmit time intervals;

mixing means for combining the adjusted transmit IF signal and the RF reference signal to produce an RF transmit signal;

amplifying means coupled to the supply voltage for amplifying the RF transmit signal to produce the RF output signal;

voltage detecting means for detecting the magnitude of the supply voltage;

temperature detecting means for detecting the temperature of the power control circuitry;

power detecting means coupled to the RF output signal for generating an output signal having a value related to the magnitude of the forward power of the RF output signal; and

control means coupled to the power detecting means for sampling the value of the output signal substantially at the end of each transmit time interval, adjusting the value of the gain control signal in response to the difference between the sampled value of the output signal and the selected power level, and storing the adjusted value of the gain control signal in the memory means, said control means further being coupled to the temperature detecting means for adjusting the gain control signal by a first predetermined

amount substantially at the beginning of each transmit time interval when the detected temperature is greater than a predetermined temperature, and said control means further being coupled to the voltage detecting means for adjusting the gain control signal by a second predetermined amount substantially at the beginning of of at least the initial transmit time interval when the detected magnitude of the supply voltage is less than a predetermined magnitude.

17. Power control circuitry responsive to a transmit signal, level control signals, and a supply voltage from a signal source for maintaining the magnitude of a radio frequency (RF) output signal at a power level selected from a plurality of power levels by the level control signals, said supply voltage having a magnitude between a predetermined minimum voltage and a predetermined maximum voltage, said power control circuitry comprising:

adjusting means having variable gain for adjusting the transmit signal during the transmit time intervals substantially in proportion to the value of the gain control signal to produce an adjusted transmit signal;

amplifying means coupled to the supply voltage for amplifying the transmit signal to produce the RF output signal;

antenna means coupled to the amplifying means for transmitting the RF output signal;

voltage detecting means for detecting the magnitude of the supply voltage;

temperature detecting means for detecting the temperature of the power control circuitry;

first power detecting means coupled to the RF output signal for generating a first output signal having a value related to the magnitude of the forward power of the RF output signal; and

control means coupled to the first power detecting means for sampling the value of the first output signal substantially at a plurality of time intervals, and adjusting the value of the gain control signal in response to the difference between the sampled value of the first output signal and the selected power level, said control means further being coupled to the temperature detecting means for adjusting the gain control signal by a first predetermined amount substantially at the beginning of each time interval when the detected temperature is greater than a predetermined temperature, and said control means further being coupled to the voltage detecting means for adjusting the gain control signal by a second predetermined amount substantially at the beginning of at least the initial time interval when the detected magnitude of the supply voltage is less than a predetermined magnitude.

18. The power control circuitry according to claim 17, further including second power detecting means coupled to the RF output signal for generating a second output signal having a value related to the magnitude of the reverse power of the RF output signal, said control means further being coupled to the second power detecting means for disabling the amplifying means when the value of the second output signal exceeds a predetermined value.

19. The power control circuitry according to claim 18, further including directional coupling means for coupling a portion of the reverse power of the RF output signal to the second detecting means.

20. The power control circuitry according to claim 17, wherein said control means includes analog to digital converting means coupled to the first detecting means, digital

to analog converting means coupled to the adjusting means, and processing means coupled to said analog to digital converting means and said digital to analog converting means, said analog to digital converting means for converting the first output signal to a digitized first output signal, said processing means sampling the digitized first output signal to sample the value of the first output signal and generating a digitized gain control signal, and said digital to analog converting means converting the digitized gain control signal to the gain control signal.

21. The power control circuitry according to claim 17, further including directional coupling means for coupling a portion of the forward power of the RF output signal to the first detecting means.

22. The power control circuitry according to claim 17, wherein said first detecting means comprises first diode detecting means and said second detecting means comprises second diode detecting means.

23. The power control circuitry according to claim 17, further including filtering means intercoupling said antenna means and said amplifying means.

24. A radio communicating via a plurality of radio channels, said radio comprising in combination:

antenna means for receiving and transmitting signals via the plurality of radio channels;

receiving means coupled to the antenna means for receiving a receive signal via one of the plurality of radio channels;

transmitting means coupled to the antenna means for transmitting a radio frequency (RF) output via one

of the plurality of radio channels, said transmitting further including power control circuitry responsive to a transmit signal, level control signals, and a supply voltage from a signal source for maintaining the magnitude of the RF output signal at a power level selected from a plurality of power levels by the level control signals, said supply voltage having a magnitude between a predetermined minimum voltage and a predetermined maximum voltage, said power control circuitry comprising:

adjusting means having variable gain for adjusting the transmit signal during the transmit time intervals substantially in proportion to the stored value of the gain control signal to produce an adjusted transmit signal;

amplifying means coupled to the supply voltage for amplifying the transmit signal to produce the RF output signal;

voltage detecting means for detecting the magnitude of the supply voltage;

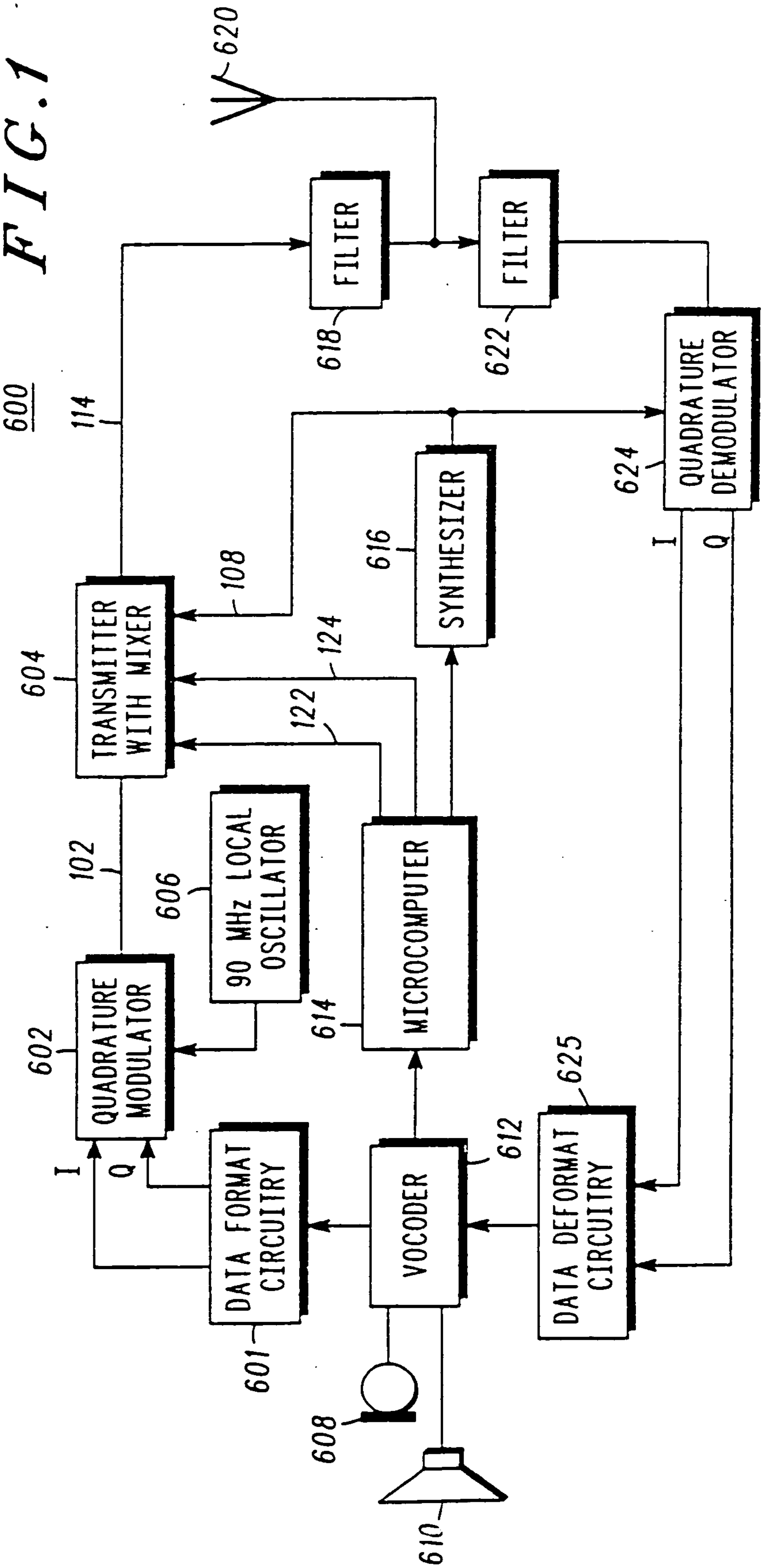
temperature detecting means for detecting the temperature of the power control circuitry;

power detecting means coupled to the RF output signal for generating an output signal having a value related to the magnitude of the forward power of the RF output signal; and

control means coupled to the power detecting means for sampling the value of the output signal substantially at a plurality of time intervals, and adjusting the value of the gain control signal in response to the difference between the sampled value of the output signal and the selected power level, said control means further being coupled to the temperature detecting means for adjusting the gain control signal by a first predetermined amount substantially at the beginning of each time interval when the detected temperature is greater than a predetermined temperature,

and said control means further being coupled to the voltage detecting means for adjusting the gain control signal by a second predetermined amount substantially at the beginning of of at least the initial time interval when the detected magnitude of the supply voltage is less than a predetermined magnitude.

FIG.1



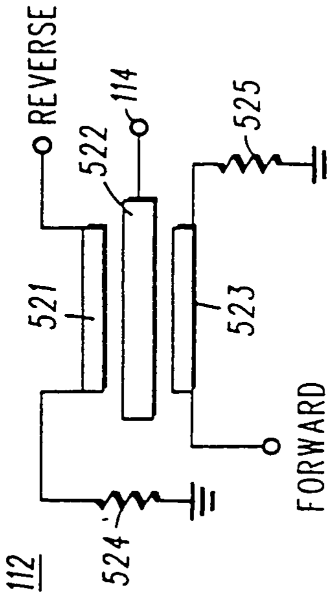


FIG.5

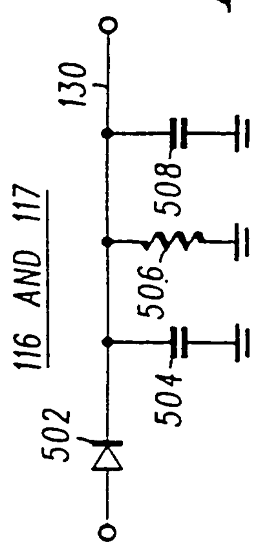


FIG.4

2/6

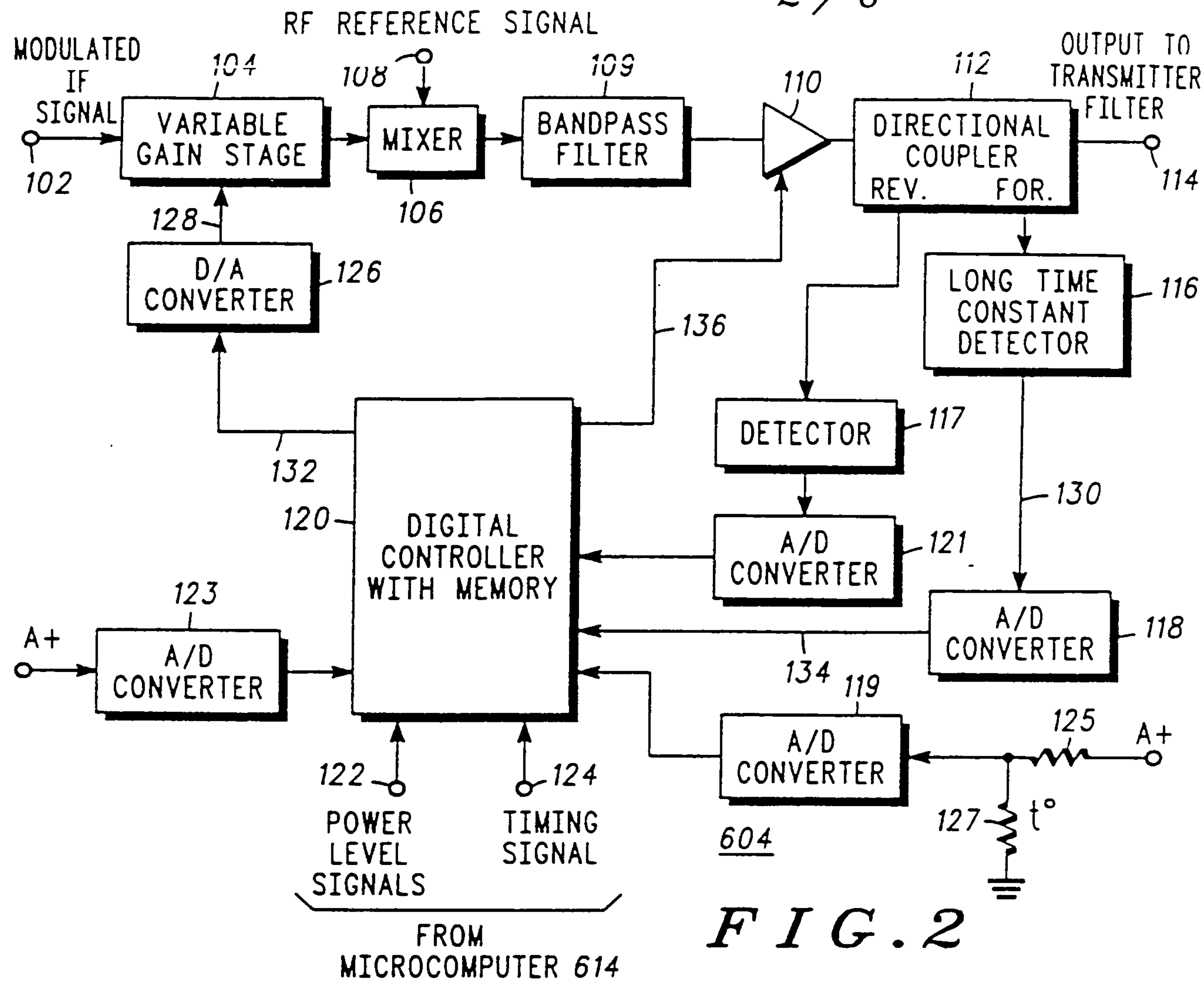

RF REFERENCE SIGNAL
MODULATED IF SIGNAL
104
108
109
110
112
OUTPUT TO TRANSMITTER FILTER
VARIABLE GAIN STAGE
MIXER
BANDPASS FILTER
DIRECTIONAL COUPLER
REV. FOR.
102
106
114
128
D/A CONVERTER
126
LONG TIME CONSTANT DETECTOR
116
136
DETECTOR
117
132
120
DIGITAL CONTROLLER WITH MEMORY
130
A/D CONVERTER
121
123
A+
A/D CONVERTER
A/D CONVERTER
118
134
119
A/D CONVERTER
125
A+
122
124
POWER LEVEL SIGNALS
TIMING SIGNAL
127
t°
604
FROM MICROCOMPUTER 614

FIG. 2

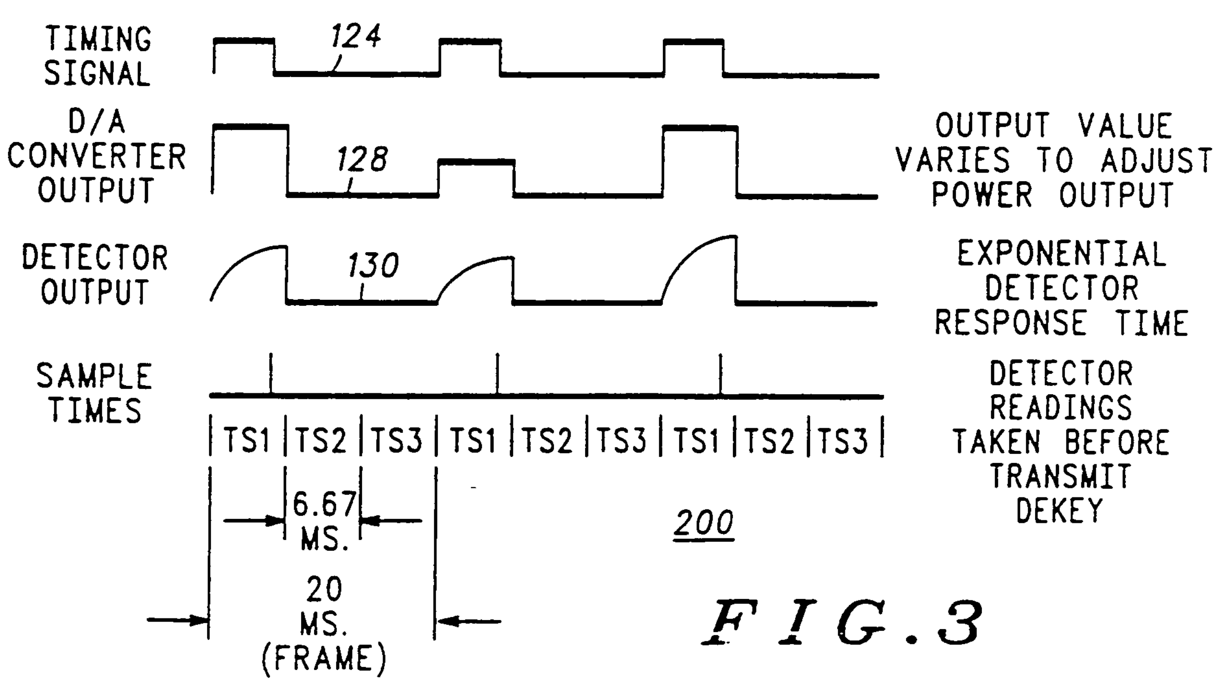

TIMING SIGNAL
124
D/A CONVERTER OUTPUT
128
OUTPUT VALUE VARIES TO ADJUST POWER OUTPUT
DETECTOR OUTPUT
130
EXPONENTIAL DETECTOR RESPONSE TIME
SAMPLE TIMES
DETECTOR READINGS TAKEN BEFORE TRANSMIT DEKEY
TS1 TS2 TS3 TS1 TS2 TS3 TS1 TS2 TS3
6.67 MS.
200
20 MS. (FRAME)

FIG. 3

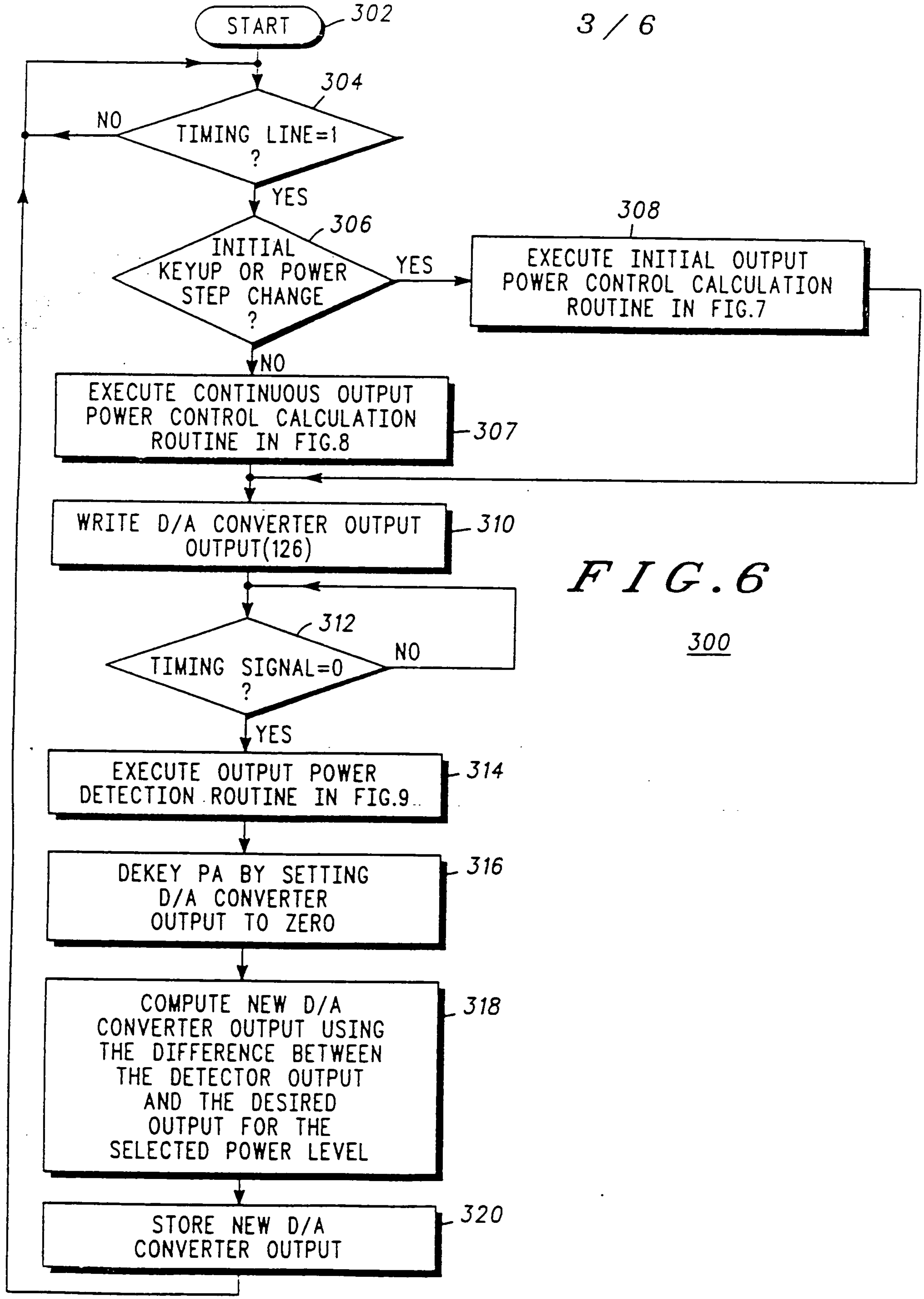

START
302
TIMING LINE=1 ?
304
NO
YES
INITIAL KEYUP OR POWER STEP CHANGE ?
306
YES
EXECUTE INITIAL OUTPUT POWER CONTROL CALCULATION ROUTINE IN FIG.7
308
NO
EXECUTE CONTINUOUS OUTPUT POWER CONTROL CALCULATION ROUTINE IN FIG.8
307
WRITE D/A CONVERTER OUTPUT OUTPUT(126)
310
TIMING SIGNAL=0 ?
312
NO
YES
EXECUTE OUTPUT POWER DETECTION ROUTINE IN FIG.9
314
DEKEY PA BY SETTING D/A CONVERTER OUTPUT TO ZERO
316
COMPUTE NEW D/A CONVERTER OUTPUT USING THE DIFFERENCE BETWEEN THE DETECTOR OUTPUT AND THE DESIRED OUTPUT FOR THE SELECTED POWER LEVEL
318
STORE NEW D/A CONVERTER OUTPUT
320

FIG.6

300

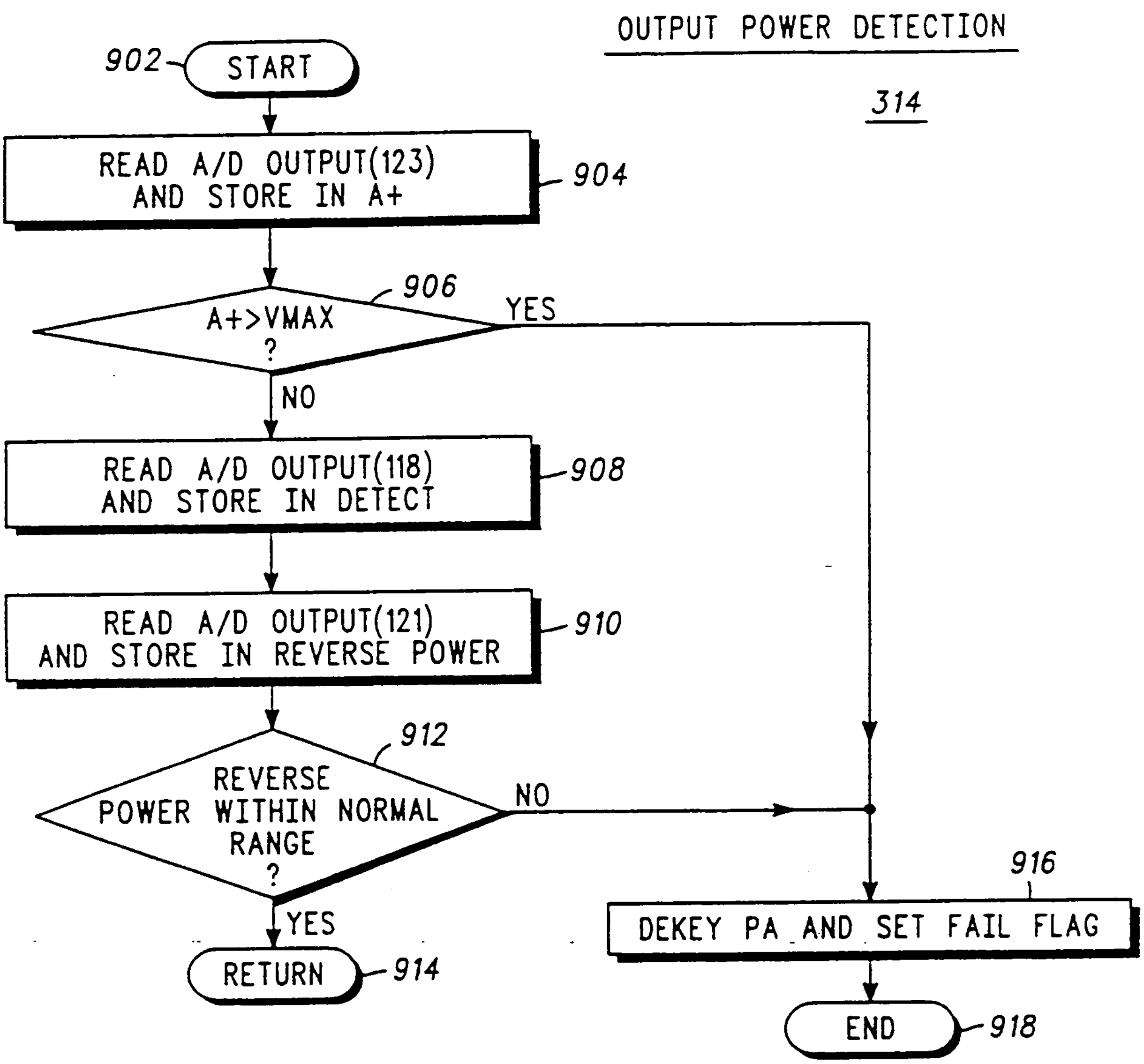

OUTPUT POWER DETECTION
314
902
START
READ A/D OUTPUT(123) AND STORE IN A+
904
906
A+>VMAX ?
YES
NO
READ A/D OUTPUT(118) AND STORE IN DETECT
908
READ A/D OUTPUT(121) AND STORE IN REVERSE POWER
910
912
REVERSE POWER WITHIN NORMAL RANGE ?
NO
YES
RETURN
914
916
DEKEY PA AND SET FAIL FLAG
END
918

FIG.9